CLAIMS

1. A video transport processor comprising:

an input for receiving one or more compressed data streams;

means for extracting video data from the compressed data streams;

means for storing the video data in an external memory; and

means for generating a start code table to index the video data stored in the external memory.

2. The video transport processor of claim 1 wherein the video data includes MPEG-2 video data, and the video transport processor further comprises means for aligning the start of SLICEs to a suitable boundary in the external memory when storing the MPEG-2 video data in the external memory.

3. A system comprising: 10, 132

a core transport processor for receiving a plurality of compressed data streams;

a first satellite transport 141, 143 processor for receiving at least one of the compressed data streams and extracting video data; and

a second satellite transport 141, 144 processor for receiving at least one of the compressed data streams and extracting audio data,

wherein the core transport processor provides data related to the compressed data streams to at least one of the

first satellite transport processor and the second satellite transport processor.

4. The system of claim 3 wherein the core transport processor, the first satellite transport processor and the second satellite transport processor are integrated on an integrated circuit chip.

5. The system of claim 3 wherein the first satellite transport processor stores the video data in a memory block and generates a start code table to index the video data stored in the memory block.

6. The system of claim 3 wherein the data related to the compressed data streams include clock reference data.

7. The system of claim 3 wherein the plurality of compressed data streams include one or more MPEG Transport streams.

8. The system of claim 7 wherein the one or more MPEG Transport streams include at least one in-band stream and at least one out-of-band stream.

9. The system of claim 5 wherein the plurality of compressed data streams include at least one MPEG-2 Transport stream.

10. The system of claim 9 further comprising an MPEG-2 video decoder for reading the video data from the memory block and decoding the video data.

11. The system of claim 9 wherein the video data includes a plurality of SLICEs, and the start code table is used to index the video data, SLICE by SLICE.

12. The system of claim 11 wherein the plurality of SLICEs include a plurality of rows of video data in the memory block, and the start code table is used to index the video data, row by row.

13. The system of claim 11 wherein the first satellite transport processor aligns the start of each of the plurality of SLICEs to a suitable boundary in the memory block when storing the video data in the memory block.

14. The system of claim 9 wherein the first satellite transport processor processes down to and including a SLICE layer of at least one MPEG-2 Transport stream.

15. The system of claim 3 wherein the video data includes at least one HDTV video.

16. A method of processing a plurality of transport streams using a system with multiple transport processors comprising the steps of:

receiving a plurality of compressed data streams at a core transport processor;

receiving at least one of the plurality of compressed data streams at a first satellite transport processor, and extracting video data;

receiving at least one of the plurality of compressed data streams at a second satellite transport processor, and extracting audio data; and

transferring data related to the compressed data streams from the core transport processor to at least one of the first satellite transport processor and the second satellite transport processor.

17. The method of processing a plurality of transport streams of claim 16 further comprising the steps of:

storing the video data in a memory block; and

generating a start code table to index the video data stored in the memory block.

18. The method of processing a plurality of transport streams of claim 16 wherein the step of transferring data related to the compressed data streams comprises the step of transferring clock reference data.

19. The method of processing a plurality of transport streams of claim 16 wherein the step of receiving the plurality of compressed data streams comprises the step of receiving one or more MPEG Transport streams.

20. The method of processing a plurality of transport streams of claim 19 wherein the step of receiving one or more

MPEG Transport streams comprises the steps of receiving at least one in-band stream and receiving at least one out-of-band stream.

21. The method of processing a plurality of transport streams of claim 17 wherein the step of receiving the plurality of compressed data streams comprises the step of receiving at least one MPEG-2 Transport stream.

22. The method of processing a plurality of transport streams of claim 21 further comprising the steps of reading the video data from the memory block and decoding the video data.

23. The method of processing a plurality of transport streams of claim 21 wherein the step of reading the video data includes the step of indexing the video data, SLICE by SLICE.

24. The method of processing a plurality of transport streams of claim 22 wherein the video data is stored in the memory block as rows, and the step of reading the video data includes the step of indexing the video data, row by row.

25. The method of processing a plurality of transport streams of claim 17 wherein the step of storing the video data comprises the step of aligning the start of each of the plurality of SLICEs to a suitable boundary in the memory block.

26. The method of processing a plurality of transport streams of claim 16 wherein the step of extracting video data comprises the step of extracting at least one HDTV video.

27. A system comprising:

a core transport processor for receiving a plurality of compressed data streams;

a satellite transport processor for receiving at least one of the compressed data streams and for extracting video data, the video data including a plurality of SLICEs;

an MPEG-2 video decoder for decoding the video data to generate decoded video data; and

a video compositor for blending the decoded video data with graphics,

wherein the satellite transport processor generates a start code table to index the video data and aligns the plurality of SLICEs to a suitable boundary.

28. The system of claim 27 wherein the core transport processor, the satellite transport processor, the MPEG-2 video decoder and the video compositor are integrated on an integrated circuit chip.

29. The system of claim 27 wherein the video data include SDTV video data.

30. The system of claim 27 wherein the video data include HDTV video data.